Amendments to the Drawings:

The attached sheets of drawings include changes to Fig. 1. The replacement sheet including Fig. 1, replaces the original sheet, including Fig. 1. As noted in the annotated sheet including Fig. 1, the descriptive label "Prior Art" has been added for clarity.

Attachments: Replacement Sheet
Annotated Sheet Showing Change

REMARKS

Claims 1, 3-17, 19-44, 46-47 and 49-122 are pending in the present application. In the Office Action dated April 13, 2007, Figure 1 was objected to under MPEP § 608.2(g) for failing to include the label "Prior Art". Claims 1, 3-12, 15-17, 19-30, 33-44, 46-47, 49-61, 64-68, 71-73, 76-78, 80-87, 90-93, 96-99 and 101-122 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of U.S. Patent No. 5,423,009 to Zhu ("Zhu"). Claims 13-14, 31-32, 62-63, 69-70, 74-75, 79, 88-89, 94-95 and 100 were rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Zhu, and further in view of U.S. Patent No. 4,443,845 to Hamilton et al. ("Hamilton").

Objections to the Drawings

Figure 1 is objected to as failing to include the label "Prior Art." Submitted herewith is a replacement Figure 1 having the label as requested by the Examiner.

Discussion of the Disclosed Embodiment

The disclosed embodiments of the invention will now be discussed in comparison to the prior art. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the prior art subject matter, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

In one disclosed embodiment, a memory system includes a memory hub controller coupled to at least one memory module having a memory hub and a number of memory devices coupled to the memory hub. The memory hub is coupled to the memory hub controller by a bus having a fixed number of lines. Command, address and data signals are coupled between the memory hub controller and the memory hub over the bus. A first data channel includes a group of lines of the bus are used for carrying data to the memory hub while the a second channel includes the remaining of lines, which carry data to the memory hub controller. During operation of the memory system, the volume of data flowing to and from the memory hub is monitored. The number of lines forming each channel is increased or decreased according to which direction has a higher volume of traffic, with the total number of lines carrying data remaining fixed. Adjustments to the number of lines may also be based on anticipated volumes of data traffic.

The novel system disclosed provides the important benefit that bottlenecks between the memory hub and memory hub controller are reduced by adapting the capacity according to current needs.

Discussion of the Cited References

Zhu discloses a system in which a device having a fixed bus width may communicate with another device having a variable bus width that can be adjusted to be equal to the fixed bus width. Disclosure in Zhu relating to a bus having a variable width includes the Abstract, which states, "In particular, a bus interface controller interfaces a host device having a host bus of a predetermined physical bus width to a slave device having a slave bus of a variable one of multiple possible logical bus widths." Zhu also states that "[i]n general, the bus mapper maps a host bus of arbitrary width to a variable width port by automatically generating multiple transfer cycles. The variable slave bus width is therefore auto-configurable, with the bus controller generating multiple transfer cycles for one master cycle request." Col. 3, lns. 42-47.

The system of Zhu provides a means for one device to conform to the fixed bus width of another device. Zhu teaches a single host bus and another device that has a variable bus to accommodate the bus of a host device. Zhu does not teach dividing a bus into variable width input and output channels. Zhu further does not teach varying the number of lines in each of the two channels according to data transfer rates, with the total number of lines remaining fixed. The width of the bus in the device of Zhu is determined only according to the host bus width.

Hamilton fails to remedy the deficiencies of Zhu as pointed out in the previous Office Action Response.

Discussion of the Claims

Turning now to the claims, none of the cited references teach, in combination with the other limitations of claim 1, a method including the step of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a communications path having a first capacity; coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a communications path having a second capacity, *where the sum of the first capacity and the second capacity is a fixed value; and altering the first capacity and the second capacity during the operation of the memory system based on the rate at which the signals are being coupled*

from the memory hub controller to the memory hub in the at least one memory module and based on the rate at which the signals are being coupled from the memory hub in the at least one memory module to the module memory hub controller." (emphasis added)

Claims 3-16 are dependent on claim 1 and are therefore allowable

With respect to claim 17, none of the cited references teach, in combination with the other limitations of the claim, the steps of "coupling data signals from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus, where N+P = M; and altering the values of N and P during the operation of the memory system based on the rate at which signals are being coupled through the bus."

Claims 19-35 are dependent on allowable claim 17 and are therefore allowable.

With respect to claim 36, none of the cited references teach, in combination with the other limitations of the claim, a memory system having "a memory hub controller having M buffers, N of the M buffers being configured as output buffers and P of the M buffers being configured as input buffers, *the values of N and P being alterable during the operation of the memory system*; ... and a bus having M signal lines each of which is coupled between a respective buffer of the memory hub controller and a respective buffer of the memory hub, *the value of M being equal to the sum of N and P and the values of N and P further being altered within a range of minimum and maximum values of N and P respectively.*" (emphasis added).

Claims 37-44 and 46 are dependent on allowable claim 36 and are therefore allowable.

With respect to claim 47, none of the cited references teach, in combination with the other limitations of the claim, a processor-based system having "a downstream bus coupled between the output port of the memory controller and the memory hub of the at least one memory module, the downstream bus having a width of M bits, *the value of M being variable to adjust that bandwidth of the downstream bus and the value of M further being alterable based on the rate at which the signals are being coupled through*; and an upstream bus coupled between the input port of the memory controller and the memory hub of the at least one memory module, *the upstream bus having a width of N bits where N is equal to a fixed value less M, the value of N being variable to adjust that bandwidth of the upstream bus and the value of N further being alterable based on the rate at which the signals are being coupled through.*" (emphasis added).

Claims 49-57 are dependent on allowable claim 47 and are therefore allowable.

With respect to claim 58, none of the cited references teach in combination with the other limitations of the claim, a method including the steps of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using a communications path having a first capacity*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using a communications path having a second capacity, where the sum of the first capacity and the second capacity is a fixed value; altering the first capacity and the second capacity during the operation of the memory system.*" (emphasis added).

Claims 59-65 depend on allowable claim 58 and are therefore allowable.

With respect to claim 66, none of the cited references teach, in combination with the other limitations of the claim, a method including the steps of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using a communications path having a first capacity*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using a communications path having a second capacity, where the sum of the first capacity and the second capacity is a fixed value; and altering the first capacity and the second capacity during the operation of the memory system based on the rate at which it is anticipated that the signals will be coupled from the memory hub controller to the memory hub in the at least one memory module and based on the rate at which it is anticipated that the signals will be coupled from the memory hub in the at least one memory module to the module memory hub controller.*" (emphasis added).

Claims 67-72 depend on allowable claim 66 and are therefore allowable.

With respect to claim 73, none of the cited references recite, in combination with the other limitations of the claim, a method including the steps of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using a communications path having a first capacity*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using a communications path having a second capacity, where the sum of the first capacity and the second capacity is a fixed value; and altering the first capacity and the second capacity during*

the operation of the memory system within a range of minimum and maximum values for the first capacity and the second capacity respectively." (emphasis added).

Claims 74-77 depend on allowable claim 73 and are therefore allowable.

With respect to claim 78, none of the cited references teach in combination with the other limitations of the claim, a method including the steps of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using a communications path having a first capacity*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using a communications path having a second capacity, where the sum of the first capacity and the second capacity is a fixed value; and manually altering the first capacity and the second capacity during the operation of the memory system.*"'

Claims 79-81 depend on allowable claim 78 and are therefore allowable.

With respect to claim 82, none of the cited references teach, in combination with the other limitations of the claim, a method including the steps of "coupling signals in a packet that includes command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using a communications path having a first capacity*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using a communications path having a second capacity, where the sum of the first capacity and the second capacity is a fixed value; and altering the first capacity and the second capacity during the operation of the memory system.*" (emphasis added).

Claim 83 depends on allowable claim 82 and is therefore allowable.

With respect to claim 84, none of the cited references teach in combination with the other limitations of the claim, a method including the steps of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using N of the M signal lines of the bus*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using P of the M signal lines of the bus, where N+P = M; and altering the values of N and P during the operation of the memory system by configuring buffers in the memory hub controller and in the memory hub of the at least one memory module as either input buffers or output buffers.*" (emphasis added).

Claims 85-92 depend on allowable claim 84 and are therefore allowable.

With respect to claim 93, none of the cited references teach, in combination with the other limitations of the claim a method including the steps of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using N of the M signal lines of the bus*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using P of the M signal lines of the bus, where N+P = M; and altering the values of N and P during the operation of the memory system, the values of N and P being within a range of minimum and maximum values of N and P respectively.*" (emphasis added).

Claims 94-98 depend on allowable claim 93 and are therefore allowable.

With respect to claim 99, none of the cited references teach, in combination with the other limitations of claim 99, a method including the steps of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus; coupling data signals from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus, where N+P = M; and manually altering the values of N and P during the operation of the memory system."

Claims 100-103 depend on allowable claim 99 and are therefore allowable.

With respect to claim 104, none of the cited references teach, in combination with the other limitations of the claim, a method including the steps of "coupling signals in a packet that includes command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using N of the M signal lines of the bus*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using P of the M signal lines of the bus, where N+P = M; and altering the values of N and P during the operation of the memory system.*" (emphasis added).

Claims 105-106 are dependent on allowable claim 104 and are therefore allowable.

With respect to claim 107, none of the cited references teach, in combination with the other limitations of the claim, a method including the steps of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using N of the M signal lines of the bus and further using a uni-directional downstream*

bus having N signal lines; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using P of the M signal lines of the bus and further using a uni-directional upstream bus having P signal lines, where N+P = M; and altering the values of N and P during the operation of the memory system.*" (emphasis added).

Claim 108 is dependent on allowable claim 107 and is therefore allowable.

With respect to claim 109, none of the cited references teach, in combination with the other limitations of the claim, a memory system including "a memory hub controller having M buffers, *N of the M buffers being configured as output buffers and P of the M buffers being configured as input buffers, the values of N and P being alterable during initialization of the memory system*...[and] a bus having M signal lines each of which is coupled between a respective buffer of the memory hub controller and a respective buffer of the memory hub, *the value of M being equal to the sum of N and P.*" (emphasis added).

Claims 110-117 depend on allowable claim 109 and are therefore allowable.

With respect to claim 118, none of the cited references teach, in combination with the other limitations of the claim, a processor-based system including "a downstream bus coupled between the output port of the memory controller and the memory hub of the at least one memory module, the downstream bus having a width of M bits, *the value of M being variable to adjust that bandwidth of the downstream bus and the value of M further being alterable based on the rate at which it is anticipated that the signals will be coupled through at least the downstream bus*; and an upstream bus coupled between the input port of the memory controller and the memory hub of the at least one memory module, *the upstream bus having a width of N bits where N is equal to a fixed value less M, the value of N being variable to adjust that bandwidth of the upstream bus and the value of N further being alterable based on the rate at which it is anticipated that the signals will be coupled through at least the upstream bus.*"

Claims 119-122 depend on allowable claim 118 and are therefore allowable

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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MGP:sp

Enclosures:
Postcard
Fee Transmittal Sheet (+ copy)
Replacement Drawing Sheet (Fig. 1, Sheet 1)
Annotated Sheet Showing Change (Fig. 1, Sheet 1)

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Annotated Sheet
Showing Changes

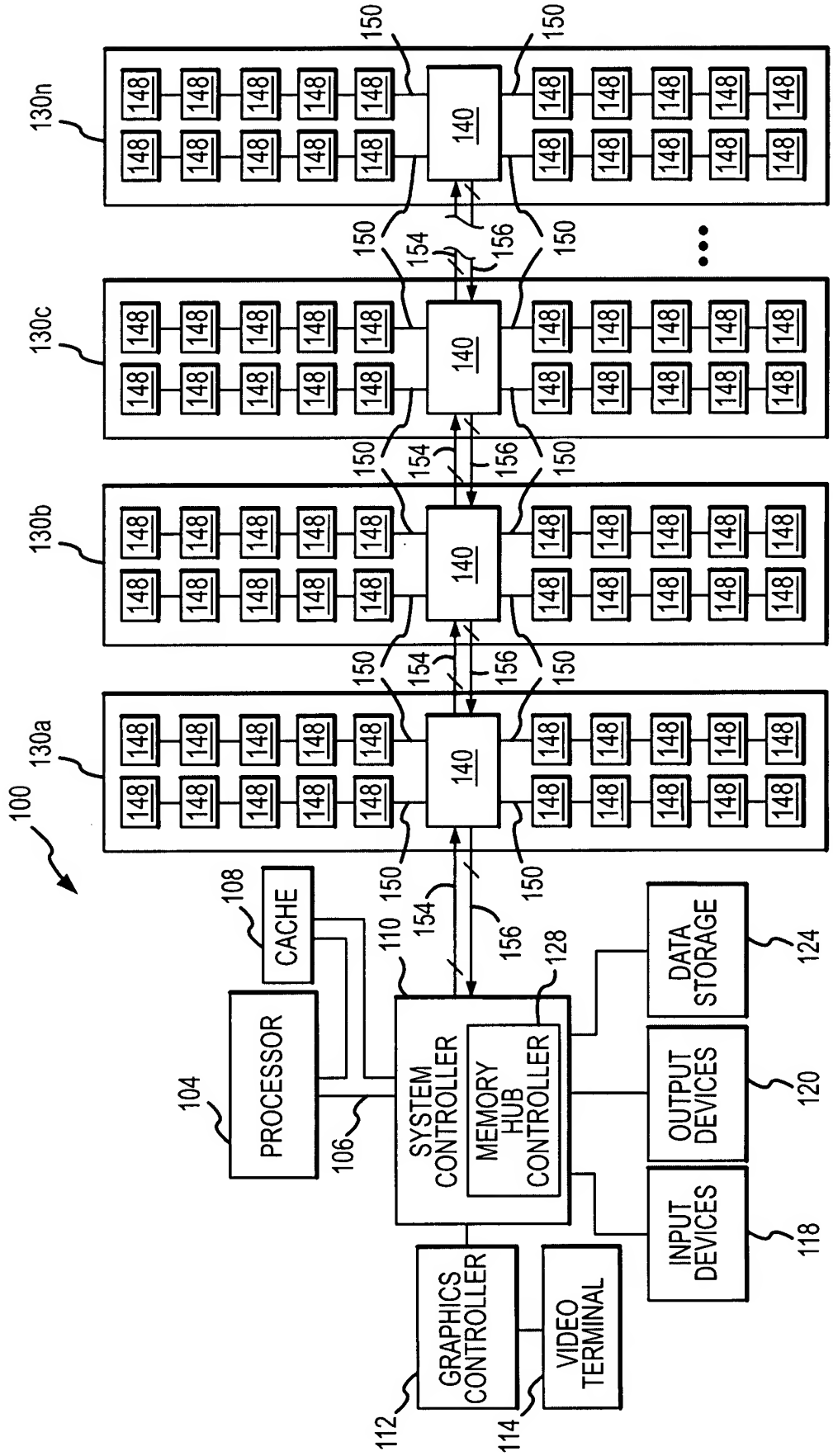

FIG.1
PRIOR ART